REMARKS

Present Status of Application – Prosecution Reopened

The Examiner is thanked for his continued indication that claims 3-7, 10-14, and 17-20 are allowable. The Office Action, however, rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent 5,883,814 to Luk (hereafter Luk). In making this rejection, the Examiner reopened prosecution (instead of answering Applicant's Appeal Brief). For the reasons set forth below, Applicant respectfully requests that the rejections be withdrawn.

Admonition against Piecemeal Examination

This is now the second time that the Examiner has reopened prosecution on these claims, citing, for the first time, the Luk patent. The Luk patent issued in 1999, and the claims of the present application have not substantive changed since the filing of this application.

In this regard, claims 3-7, 10-14, and 17-20 have always been allowed (throughout the entire prosecution of this application). To date, however, claims 1, 2, 8, 9, 15, and 16 have been consistently rejected. The latest Office Action applies Luk, for the first time, to reject these claims, and Luk is now the sixth patent that the Examiner has cited to reject these claims. The following listing chronologically summarizes the prosecution history of this application:

1.	Office Action mailed 8-14-01	→	Applied U.S. Patent 6,053,366
2.	Office Action mailed 12-5-01	→	Applied U.S. Patent 5,446,674
3.	Office Action mailed 4-24-02	→	Continued to apply U.S. Patent 5,446,674
4.	Applicant Appealed rejection		
5.	Office Action mailed 1-15-03	→	Applied U.S. Patent 5,844,818
6.	Office Action mailed 6-4-03	→	Applied U.S. Patent 6,499,129
7.	Office Action mailed 10-6-03	→	Continued to apply U.S. Patent 5,844,818
8.	Office Action mailed 3-18-04	→	Applied U.S. Patent 5,936,868

9. Applicant Appealed rejection
10. Office Action mailed 4-4-05 → Now applies U.S. Patent 5,883,814

The Patent Office has established rules against such piecemeal examination practices (see e.g. MPEP 707.07(g)). Such practices impose undue delay and expenses on the Applicants, which has now unfortunately occurred in this application. Notwithstanding, Applicants have endeavored (herein) to respond in such a way as to cooperatively advance the prosecution of this application.

Summary of Present Application

The present application is directed to a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program, which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field-effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable level of noise immunity.

Each gate typically comprises a plurality of FETs, usually an NFET and a PFET, and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise-level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs, either through calculation or simulation. The rules checker program compares the determined noise levels with the threshold values and

uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Discussion of Office Action Rejections

Applicant respectfully traverses the rejections and submits that they should be withdrawn.

Fundamental Distinction of Claimed Invention over Luk

Each independent claim of the present application defines, in some way, the analysis of the widths of the field effect transistors (that make up the gate) to determine whether or not the gate has an acceptable noise immunity. Luk fails to disclose any such teaching. In fact, the Office Action admits that Luk does not teach this. In this regard, the second and third paragraphs on page 3 of the Office Action state:

> ... Luk does not expressly disclose the claimed "gate width" of the gate transistors under rule checking (DRC) program.
>
> Practitioner in the art at the time of the invention was made would have found Luk chip design verification above would include the claimed gate width because the design rule check program checks CMOS gate parameters in the gate layout such as gate transistor width, size, etc. in determination of the gate noise immunity.

This rejection is improper, as the Examiner has substituted his own subjective judgment in place of a claimed feature that is required to be taught in the prior art. In this regard, Applicant references MPEP § 2143.03, which provides:

> **2143.03 All Claim Limitations Must Be Taught or Suggested**
>
> To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent

> claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

The Office Action has failed to follow this requirement. The claimed feature of analyzing the widths of the field effect transistors (that make up the gate) to determine whether or not the gate has an acceptable noise immunity is not disclosed (or inherent) in Luk. Furthermore, the suggestion of such a feature is not disclosed in Luk, and the Office Action has admitted as much.

Simply stated, there is no statute, regulation, or even MPEP rule that permits the Examiner to substitute his subjective judgment to account for a claimed feature of the invention. For at least this reason, the Office Action's reliance on Luk is fundamentally flawed and all rejections based on Luk should be withdrawn.

Discussion of Rejection of Claims 1, 2, 15, and 16

The Office Action rejected independent claims 1 and 15 under 35 U.S.C. § 103(a), as allegedly unpatentable over U.S. Patent 5,883,814 to Luk et al.. Applicant respectfully traverses this rejection for at least the reasons that follow.

Turning first to independent claim 1, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

Likewise, claim 15 recites:

> 15. A computer-readable medium containing a rules checker computer program, the computer program ***evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the gate comprising

> at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
>
> ***code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of independent claims 1 and 15 for at least the reason that the cited art fails to disclose or teach at least the features emphasized above.

The Office Action alleged that Luk teaches these features (or an obvious variant thereof). Applicant respectfully disagrees. First, and as Applicant pointed out above, the Office Action rejection is flawed insofar as it does not cite a proper teaching or suggestion within Luk for the claimed feature of "***analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***." For at least this reason, the rejection should be withdrawn.

In addition, and as an independent basis for patentability, Luk is directed to a layout compiler for system-on-chip layout compilations. There is no teaching within Luk of the evaluation of any gate or node to ascertain or evaluate noise immunity. The second paragraph on page 3 of the Office Action generally alleges this teaching within Luk, citing Figs. 9 and 14, and column 9, lines 15-50 and col. 10, lines 12-57. Applicant respectfully disagrees. In this regard, Fig. 9 of Luk is simply a high-level block diagram of a system-on-chip design system, and includes no teaching (whatsoever) with regard to any noise immunity analysis. Similarly, Fig. 14 of Luk is a flow diagram of the layout compilation of integrated logic/DRAM chips (see col. 3, lines 1-2), and includes no teaching (whatsoever) with regard to any noise immunity analysis. Likewise, the textual description in Luk offers no relevant teaching with respect to any noise immunity analysis. In fact, the only teaching within Luk as to "noise" appears to be the teaching epitomized in col. 5, lines 34-36, which states:

> The methods described here address the noise problem related to the integration of logic macros and DRAM macros onto the same silicon chip. When DRAM and logic are placed on different chips, the dI/dt switching noises due to the logic circuits are isolated from the DRAM cells and sense amplifier. When logic macros and DRAM macros are placed on the same chip, the switching noises from the logic circuits can propagate/couple through the power supply buses to affect the proper operations of the DRAM circuits, due to the voltage degradation of the DRAM voltage supply. Special structure of decoupling capacitance and routing of the power buses are described (hereinafter with reference to FIG. 11 and FIG. 14) to isolate the noise coupling between the logic and DRAM circuits.

The isolation of noise coupling between logic circuits and DRAM cells is not the same as the analysis of a node or gate to assess whether the analyzed node or gate has an acceptable level of noise immunity, as specifically claimed by the pending claims. Simply stated, Luk does not teach or disclose ***analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***. Consequently, the rejections to independent claims 1 and 15 should be withdrawn.

As rejected claims 2 and 16 depend from independent claims 1 and 15, the rejections to these claims should be withdrawn for at least the same reason.

Discussion of Rejection of Claims 8 and 9

The Office Action also rejected claims 8 and 9 under 35 U.S.C. § 102(e), as allegedly obvious over Luk. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 8 recites:

> 8. A method ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the method comprising the steps of:
>
> receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and

> ***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the reason that Luk fails to disclose or teach either of the features emphasized above.

The Office Action rejected claim 8, relying on the same portions of Luk that the Office Action relied upon in rejecting claim 1. In this regard, the Office Action relied principally upon the teachings in columns 7 and 8 of the Luk patent. Simply stated, and for the same reasons discussed in connection with claims 1 and 15 above, Luk does NOT teach at least the features of claim 8 that are emphasized above (i.e., "evaluating a gate to determine whether or not the gate has an acceptable immunity to noise" or "analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity."

Consequently, and for the same reasons set forth in connection with claim 1, Applicant respectfully submits that the rejection of claims 8 is misplaced and should be withdrawn. For at least these same reasons, claim 9, which depends from claim 8, patently defines over Luk as well.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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Please continue to send all future correspondence to:

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